ARUNACHALAM P

RTL Design Engineer · FPGA Developer

📍 Chennai, India · 📞 +91 6383050389 · arunachalam862005@gmail.com
GitHub: github.com/Arunachalam-212223060022 · LinkedIn: linkedin.com/in/arunachalam-p-12445b290

PROFESSIONAL SUMMARY

ECE undergraduate (2023–2027) specialising in **RTL Design, FPGA Development, and SoC Architecture** with two industry internships and national hackathon recognition. Proficient across the full RTL-to-gates flow — synthesis, STA, timing closure, DFT, and low-power analysis — using **Synopsys** and **Cadence** EDA toolchains. Delivered All India Rank 17 at NIT Jamshedpur and Finalist recognition at SAKEC × ChipMonk, with measurable PPA improvements across every project.

TECHNICAL SKILLS

HDL & Programming: Verilog, SystemVerilog, C, C++, Python, Embedded C, TCL, Shell

ASIC & VLSI: Logic Synthesis, STA, RTL-to-Gates, Timing Analysis, Power Analysis, Semiconductor Design Flow

EDA Tools: Cadence: Genus, Innovus, NC-Launch, Virtuoso (basic) | Synopsys: Design Compiler, VCS, Verdi, PrimeTime

Processor & Arch: RISC-V (RV32I), 5-Stage Pipeline, SoC Design, Memory-Mapped I/O, Interrupt Handling, QNX RTOS

Embedded & Tools: ESP32, Arduino, PCB Design, Proteus, LTspice

RTL & Verification: RTL/FSM Design, Functional Verification, Self-Checking Testbenches, STA, Timing Closure

Physical Design: Floorplanning, Placement, CTS, Routing (Fundamentals), P&R Flow Awareness

FPGA & SoC: Xilinx Vivado, Vitis HLS, Quartus Prime, PYNQ, FPGA Prototyping, HW-SW Co-Design

Protocols: AXI4, APB, UART, SPI, I2C, GPIO, Wishbone

Dev Tools: Git, GitHub, Linux, VS Code

WORK EXPERIENCE

VLSI Design Intern · Codec Technology, Chennai
Nov 2024 – Jan 2025

- **Designed, synthesised, and verified** an FPGA traffic-light controller in Vivado (RTL → synthesis → implementation → STA), reaching **Fmax > 150 MHz** within 4 weeks.
- **Cut debug time by 30%** via systematic RTL schematic checks and automated timing-constraint files; handled clock-domain crossing between RTL and I/O blocks, eliminating metastability issues.
- Communicated timing analysis and synthesis trade-offs to senior staff in 3-engineer design reviews.

Engineering Intern · NSIC Technical Services Centre, Chennai
Jul 2024 – Sep 2024

- Designed and simulated mixed-signal circuits in Proteus; resolved **5 component faults** via structured diagnostics, delivering prototypes meeting all functional specs.
- **Reduced estimated dynamic power by 12%** in key sub-circuits through low-power design techniques and power analysis.

Independent Study / Research · Self-Directed
Feb 2025 – Present

- Pursued advanced FPGA, SoC, and ASIC design through national hackathons (NIT Jamshedpur, SAKEC × ChipMonk, ARM Bharat) and NIELIT/GUVI certifications; delivered three major hardware projects with published PPA results.

PROJECTS

RISC-V Soft-Core SoC on FPGA with Integrated Peripheral Subsystems
Oct 2024 – Jan 2025

Verilog · Vivado · Artix-7 / Zynq-7020

- **Designed** a complete RV32I 5-stage pipelined processor with UART, SPI, I2C, GPIO, Timer, and Interrupt Controller; developed a UVM-based verification environment covering all processor modules, achieving **100% functional coverage** across 200+ self-checking vectors.
- **Implemented** AMBA/APB/Wishbone bus interconnect; created XDC constraint files to meet timing closure with **zero violations**. DFT + scan-chain insertion (98% coverage); PrimeTime power analysis achieved **12% dynamic power reduction**.

FPGA Edge-Analytics IP Core (SEAP-1)
🏆 **Finalist — SAKEC × ChipMonk Hackathon 2025** *Feb 2025 – Mar 2025*

Verilog · Vivado · Spartan-7 · PYNQ-Z2

- **Architected** a pipelined 5-stage IP (moving-avg → 64-pt FFT → feature extractor → anomaly detector → decision) at **100 MHz**, ~6.8 µs latency, **< 5% FPGA resources** (~2,000 LUTs, 7 DSPs).
- **Achieved** zero timing failures across **8,801 endpoints**, 69/69 tests passing, multi-board deployment with zero RTL changes; **15% power reduction** via HLS-stage low-power techniques.

Hardware-Accelerated CNN Inference System **ARM Bharat AI SoC Hackathon 2025** *Apr 2025 – May 2025*
Vitis HLS · C++ · Vivado · Zynq-7020

- **Designed** an ARM Cortex-A9 + FPGA CNN pipeline on Zynq-7020 via AXI-HP DMA, achieving **~6.6× speedup**, **~2× power reduction**, ~150 ms deterministic latency via full PS-PL HW-SW co-design.

ADAS Safety Monitor & FPGA Power Management 🏆 **All India Rank 17 — VLSI For All @ NIT Jamshedpur** *Jun 2025 – Aug 2025*
Verilog FSM · LSTM · Vivado

- **ADAS:** LSTM hazard classifier feeding a Verilog FSM priority-interrupt controller for microsecond-latency Warning/Emergency/Critical responses; hardware-verified with LED indication.
- **Power Mgmt:** LSTM workload predictor driving Dynamic Frequency Scaling via programmable clock divider to reduce FPGA dynamic power.

AWARDS & ACHIEVEMENTS

- **All India Rank 17** — VLSI For All @ NIT Jamshedpur (ADAS Safety Monitor & FPGA Power Management)
- **Finalist** — SAKEC × ChipMonk FPGA Hackathon 2025 (FPGA Edge-Analytics IP Core, SEAP-1)
- **Selected Competitor** — ARM Bharat AI SoC Hackathon 2025 (Hardware-Accelerated CNN Inference System)

LEADERSHIP & ACTIVITIES

- **Core Member, Saveetha Speakers Forum** — Student-run science & humanities forum; organised and coordinated 10+ campus events.
- **Part-Time Academic Mentor** — Teach Physics, Chemistry, and Maths to Class 10–12 students.

EDUCATION

B.E. Electronics & Communication Engineering *2023 – 2027*
Saveetha Engineering College, Chennai · **CGPA: 8.1 / 10** (up to 5th Sem)

Higher Secondary Certificate (Class XII) *2023*
DAV MHSS, Chennai · 81%

CERTIFICATIONS

RTL Design and Verification	· GUVI × HCL (Google Education Partner, ISO 9001)	*May 2026*
VLSI for Beginners	· NIELIT Calicut (MeitY) · OLC 41329	*Oct 2025*
Embedded Systems for Beginners	· NIELIT Calicut (MeitY) · OLC 28971	*Aug 2025*
Introduction to Industry 4.0 & IIoT	· NPTEL	*May 2025*
Digital Communication Fundamentals	· IEM / MindLuster	*May 2025*